FIG. 1

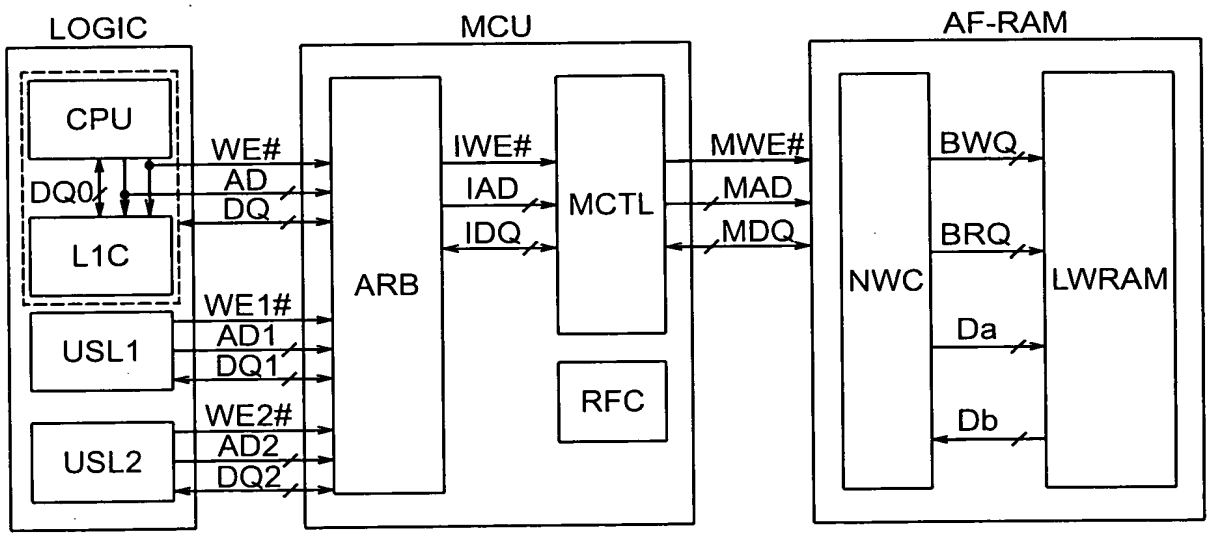

LOGIC
MCU
AF-RAM
CPU
DQ0
L1C
USL1
USL2
WE#
AD
DQ
WE1#
AD1
DQ1
WE2#
AD2
DQ2
ARB
IWE#
IAD
IDQ
MCTL
RFC
MWE#
MAD
MDQ
NWC
BWQ
BRQ
Da
Db
LWRAM

FIG. 2A

READ ACCESS,CACHE HIT

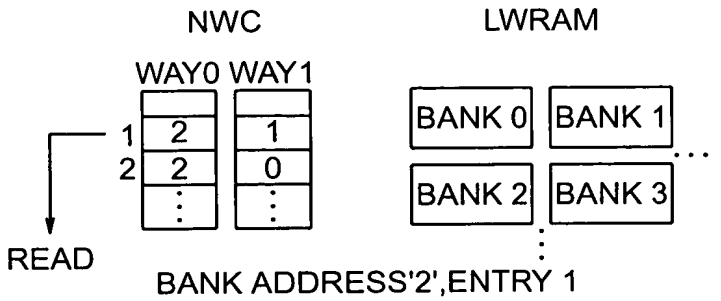


FIG. 2B

READ ACCESS,CACHE MISS

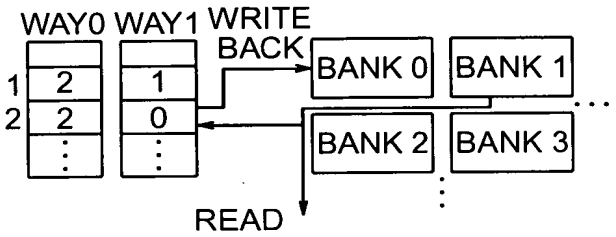


FIG. 2C

WRITE ACCESS,CACHE HIT

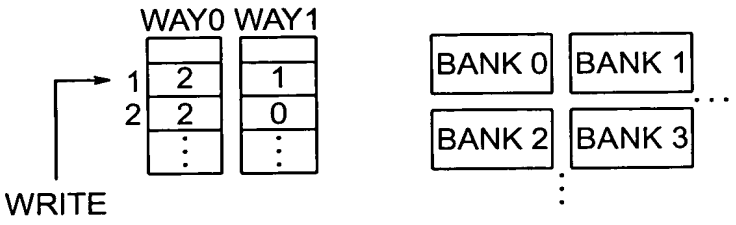


FIG. 2D

WRITE ACCESS,CACHE MISS

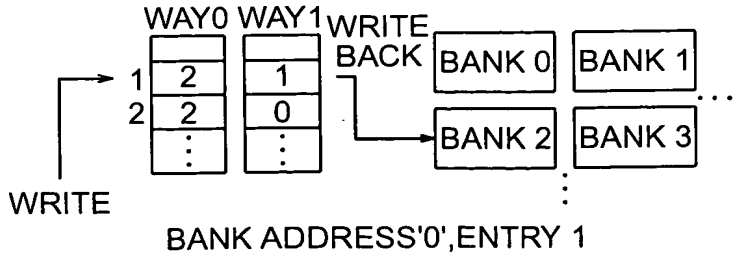
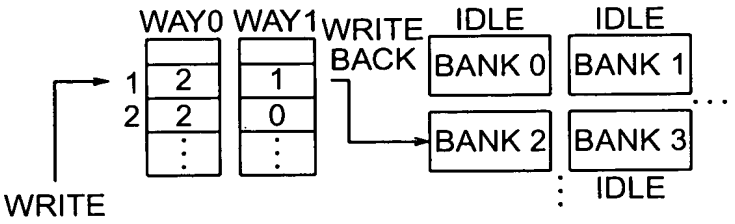


FIG. 3A

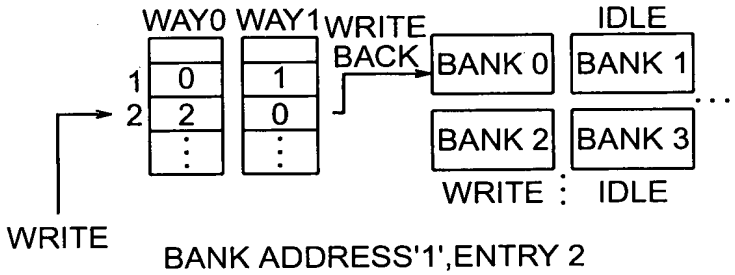
CYCLE #1:WRITE ACCESS,CACHE MISS



BANK ADDRESS'0',ENTRY 1

FIG. 3B

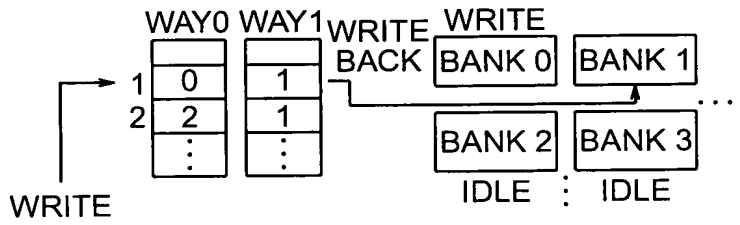
CYCLE #2:WRITE ACCESS,CACHE MISS



BANK ADDRESS'1',ENTRY 2

FIG. 3C

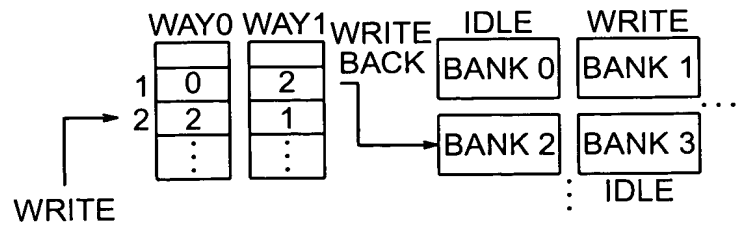
CYCLE #3:WRITE ACCESS,CACHE MISS



BANK ADDRESS'2',ENTRY 1

FIG. 3D

CYCLE #4:WRITE ACCESS,CACHE MISS



BANK ADDRESS'0',ENTRY 2

FIG. 4A

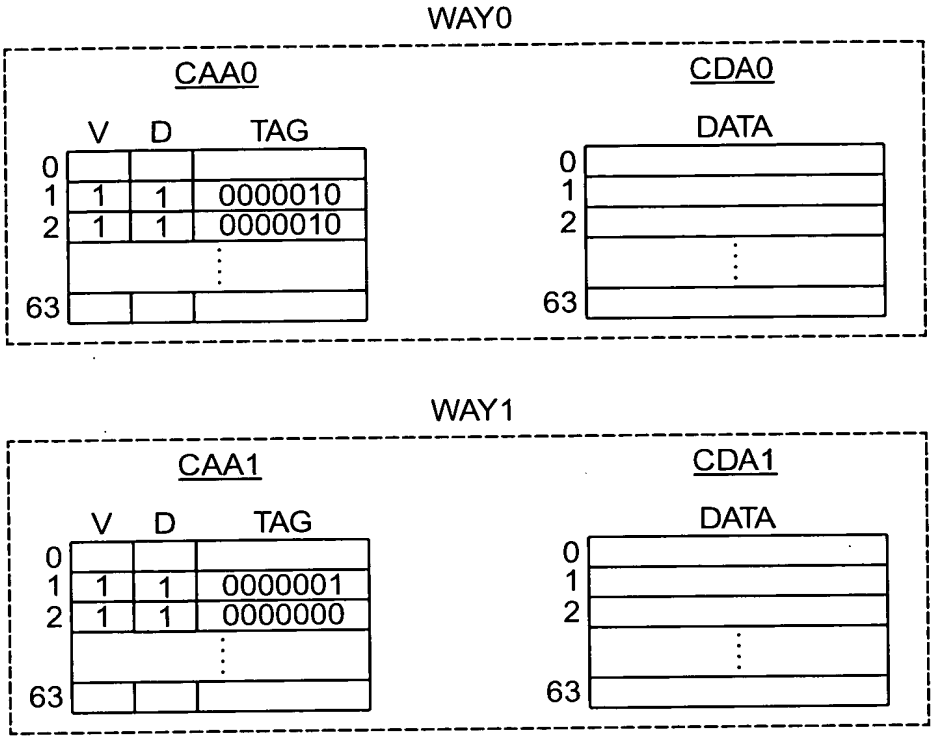

WAY0
CAA0
CDA0
V
D
TAG
DATA
0
1
2
63
1
1
0000010
1
1
0000010
WAY1
CAA1
CDA1
V
D
TAG
DATA
0
1
2
63
1
1
0000001
1
1
0000000

FIG. 4B

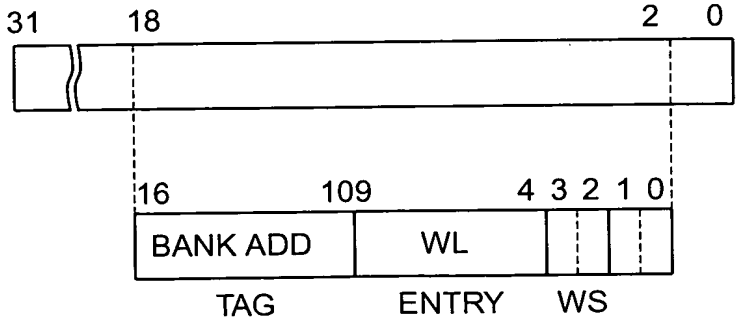

31
18
2
0
16
109
4 3 2 1 0
BANK ADD
WL
TAG
ENTRY
WS

FIG. 5

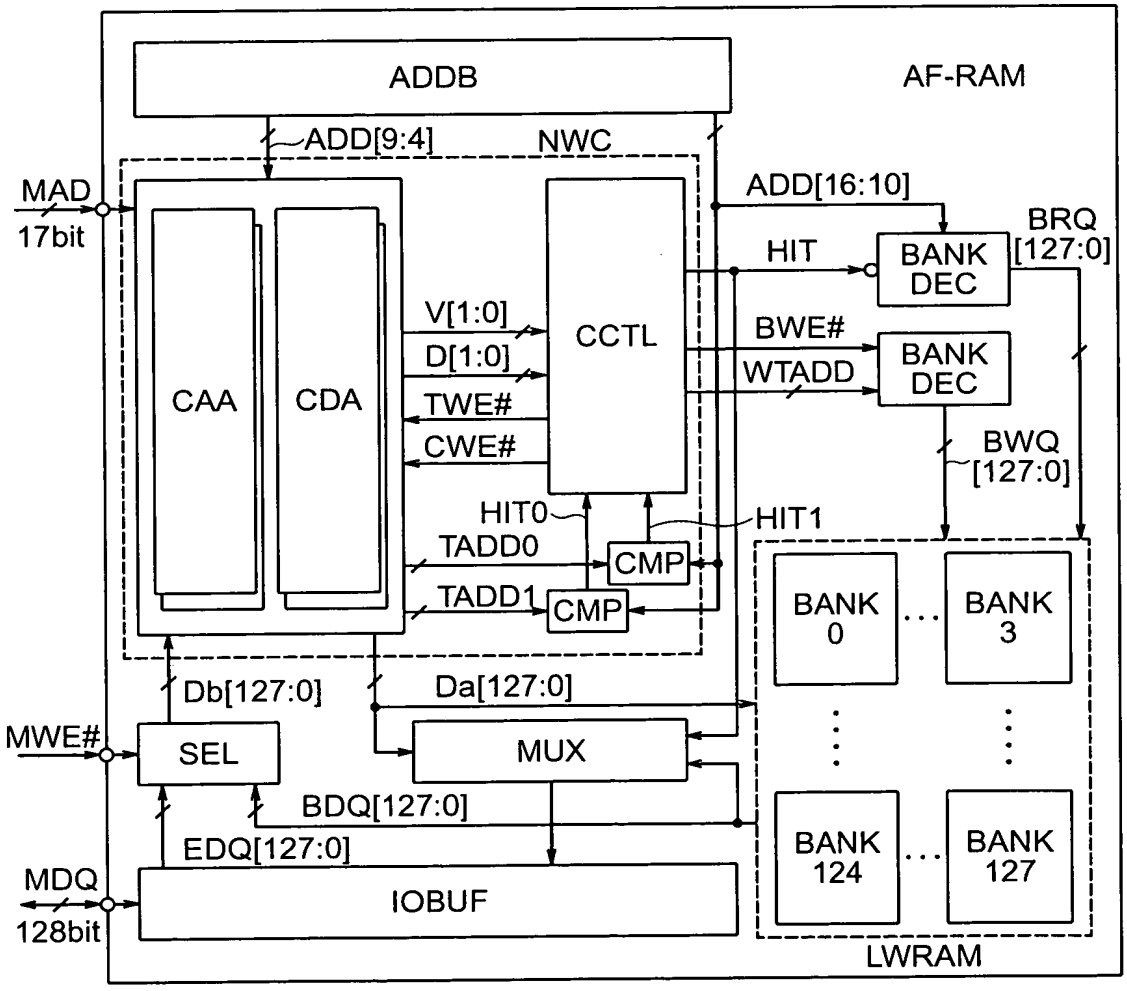

ADDB
AF-RAM
ADD[9:4]
NWC
MAD
17bit
ADD[16:10]
BRQ
[127:0]
HIT
BANK
DEC
CAA
CDA
V[1:0]
D[1:0]
TWE#
CWE#
CCTL
BWE#
WTADD
BANK
DEC
BWQ
[127:0]
HIT0
HIT1
TADD0
CMP
TADD1
CMP
BANK
0
BANK
3
Db[127:0]
Da[127:0]
MWE#
SEL
MUX
BDQ[127:0]
EDQ[127:0]
BANK
124
BANK
127
MDQ
128bit
IOBUF
LWRAM

FIG. 6

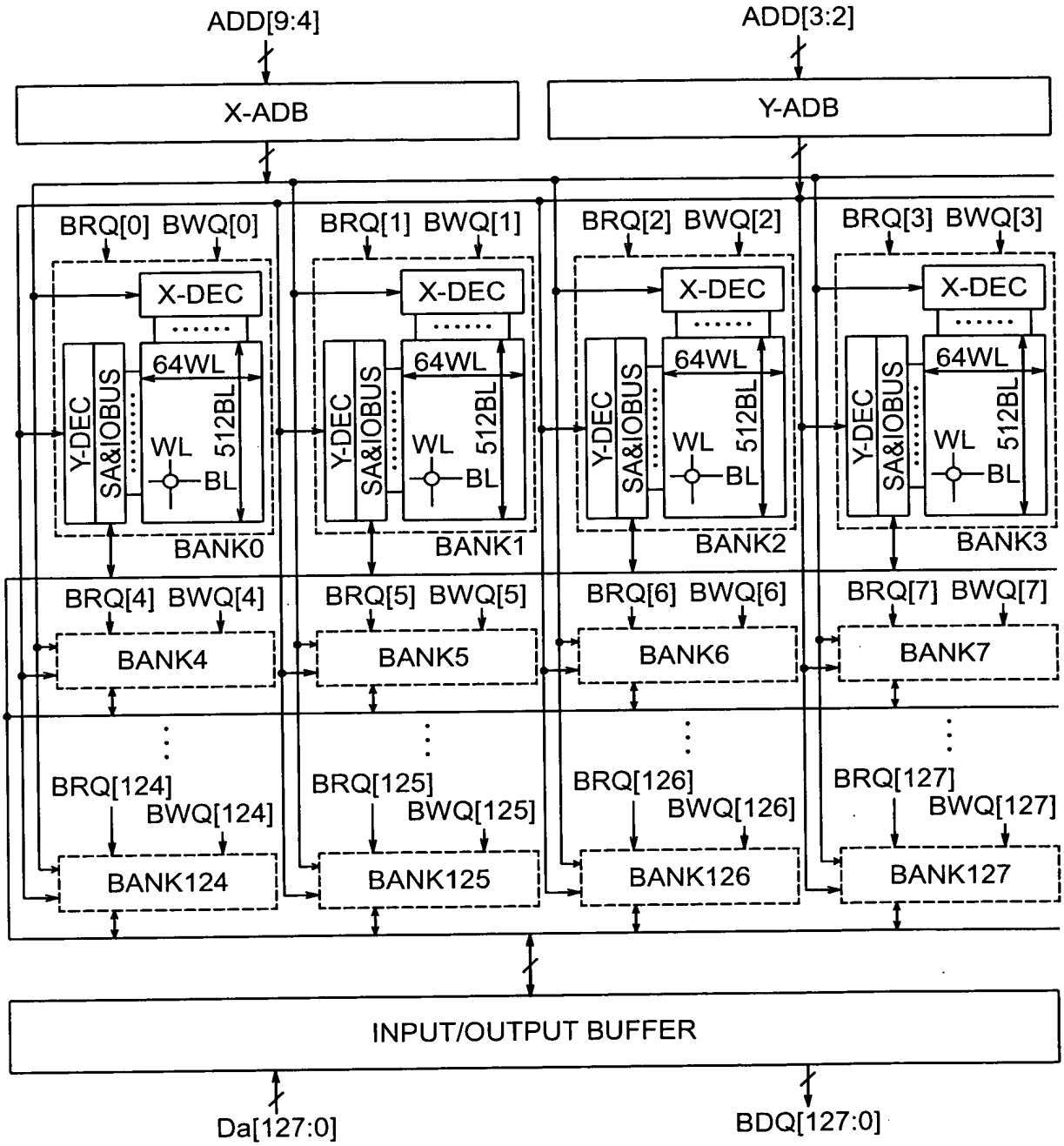

ADD[9:4]
ADD[3:2]
X-ADB
Y-ADB
BRQ[0] BWQ[0]
BRQ[1] BWQ[1]
BRQ[2] BWQ[2]
BRQ[3] BWQ[3]
X-DEC
Y-DEC
SA&IOBUS
64WL
512BL
WL
BL
BANK0
BANK1
BANK2
BANK3
BRQ[4] BWQ[4]
BRQ[5] BWQ[5]
BRQ[6] BWQ[6]
BRQ[7] BWQ[7]
BANK4
BANK5
BANK6
BANK7
BRQ[124]
BWQ[124]
BRQ[125]
BWQ[125]
BRQ[126]
BWQ[126]
BRQ[127]
BWQ[127]
BANK124
BANK125
BANK126
BANK127
INPUT/OUTPUT BUFFER
Da[127:0]
BDQ[127:0]

FIG. 7A

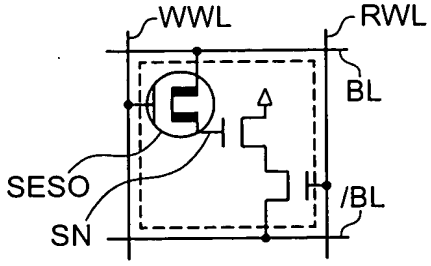

WWL
RWL
BL
SESO
/BL
SN

FIG. 7B

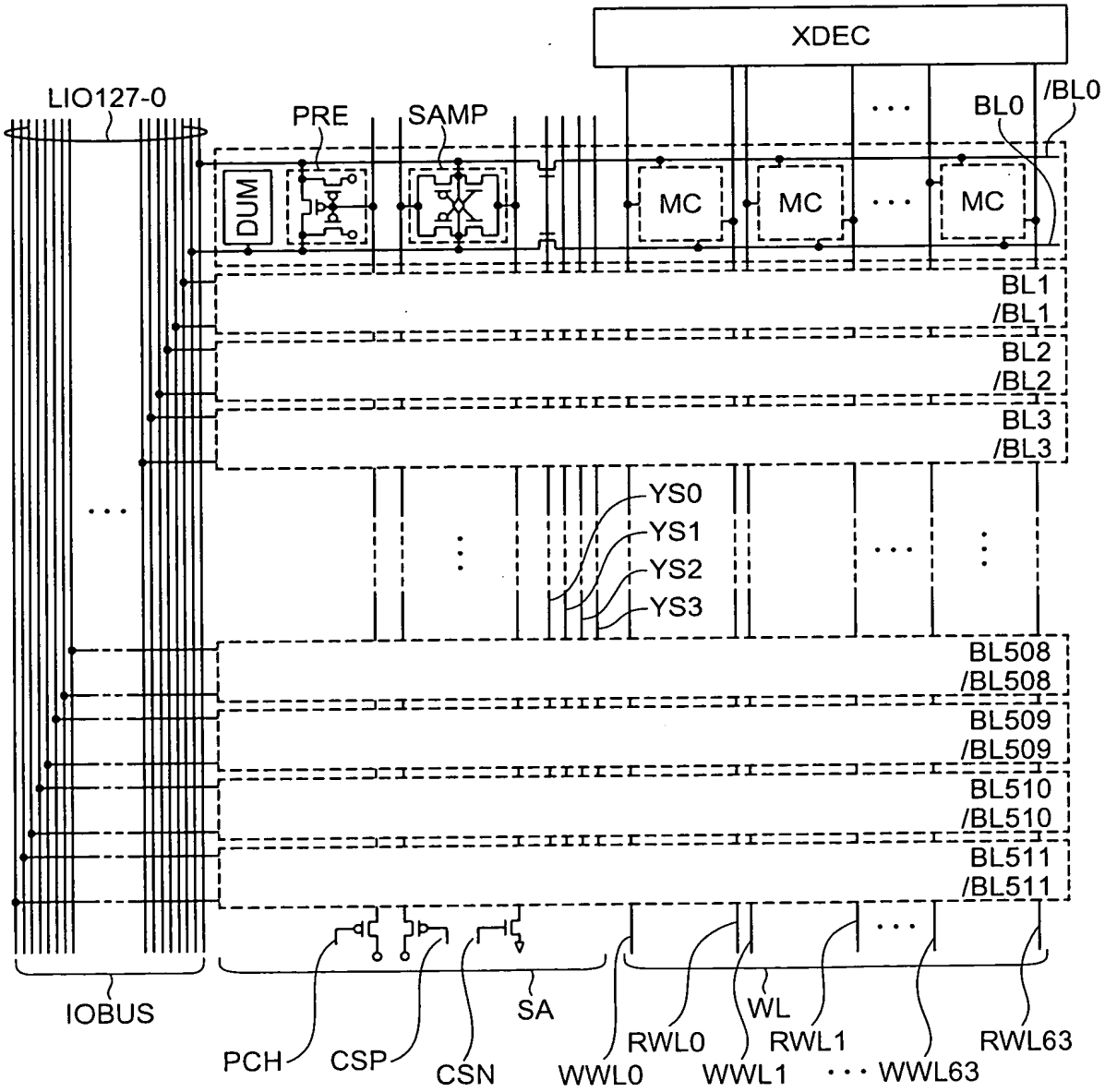

XDEC
LIO127-0
PRE
SAMP
DUM
MC
MC
MC
BL0
/BL0
BL1
/BL1
BL2
/BL2
BL3
/BL3
YS0
YS1
YS2
YS3
BL508
/BL508
BL509
/BL509
BL510
/BL510
BL511
/BL511
IOBUS
PCH
CSP
CSN
SA
WWL0
RWL0
WWL1
WL
RWL1
WWL63
RWL63

FIG. 8A

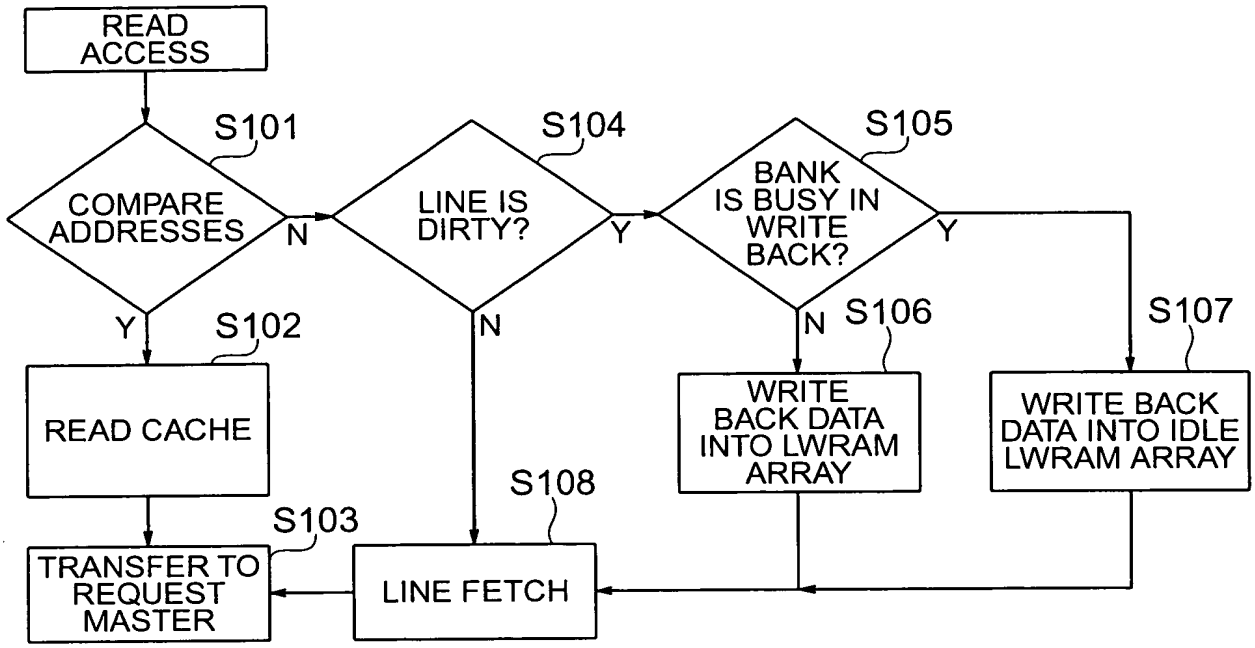

READ ACCESS
S101
COMPARE ADDRESSES
N
S104
LINE IS DIRTY?
Y
S105
BANK IS BUSY IN WRITE BACK?
Y
Y
S102
READ CACHE
N
S106
WRITE BACK DATA INTO LWRAM ARRAY
S107
WRITE BACK DATA INTO IDLE LWRAM ARRAY
S108
S103
TRANSFER TO REQUEST MASTER
LINE FETCH

FIG. 8B

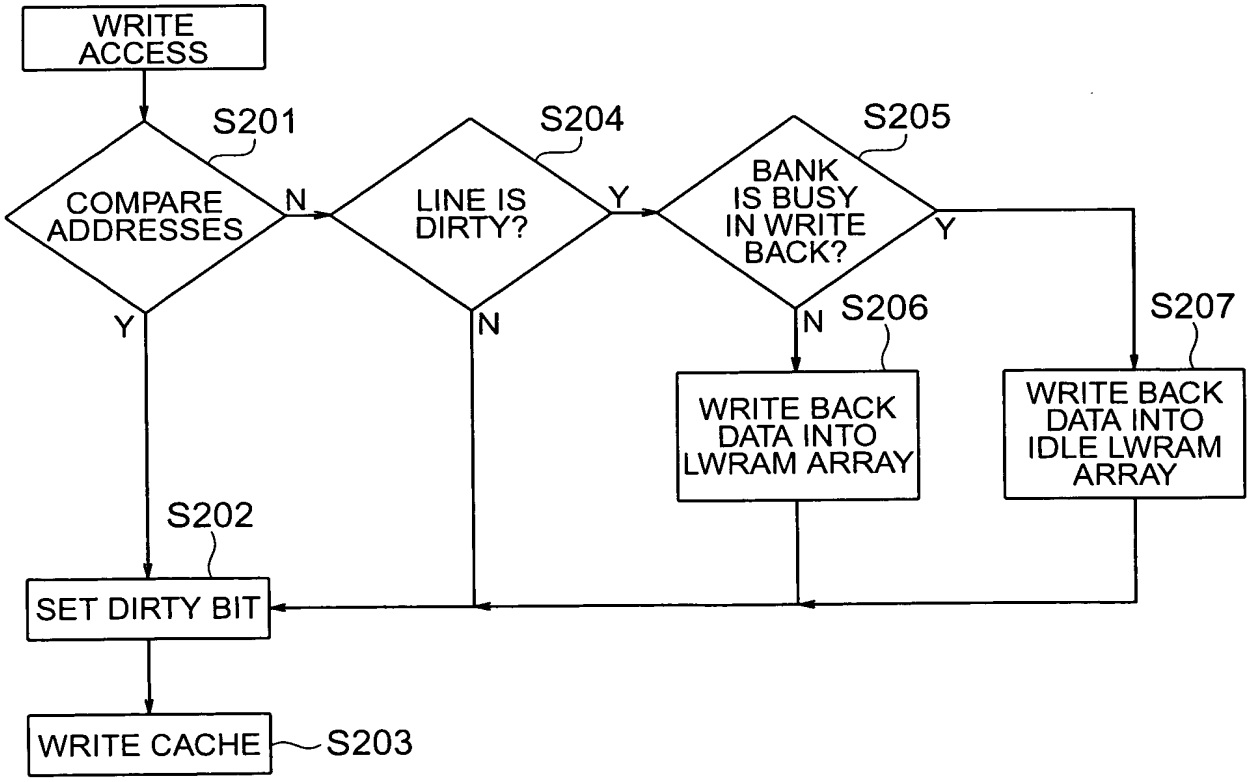

WRITE ACCESS
S201
COMPARE ADDRESSES
N
S204
LINE IS DIRTY?
Y
S205
BANK IS BUSY IN WRITE BACK?
Y
Y
S206
WRITE BACK DATA INTO LWRAM ARRAY
N
S207
WRITE BACK DATA INTO IDLE LWRAM ARRAY
S202
SET DIRTY BIT
WRITE CACHE
S203

FIG. 9

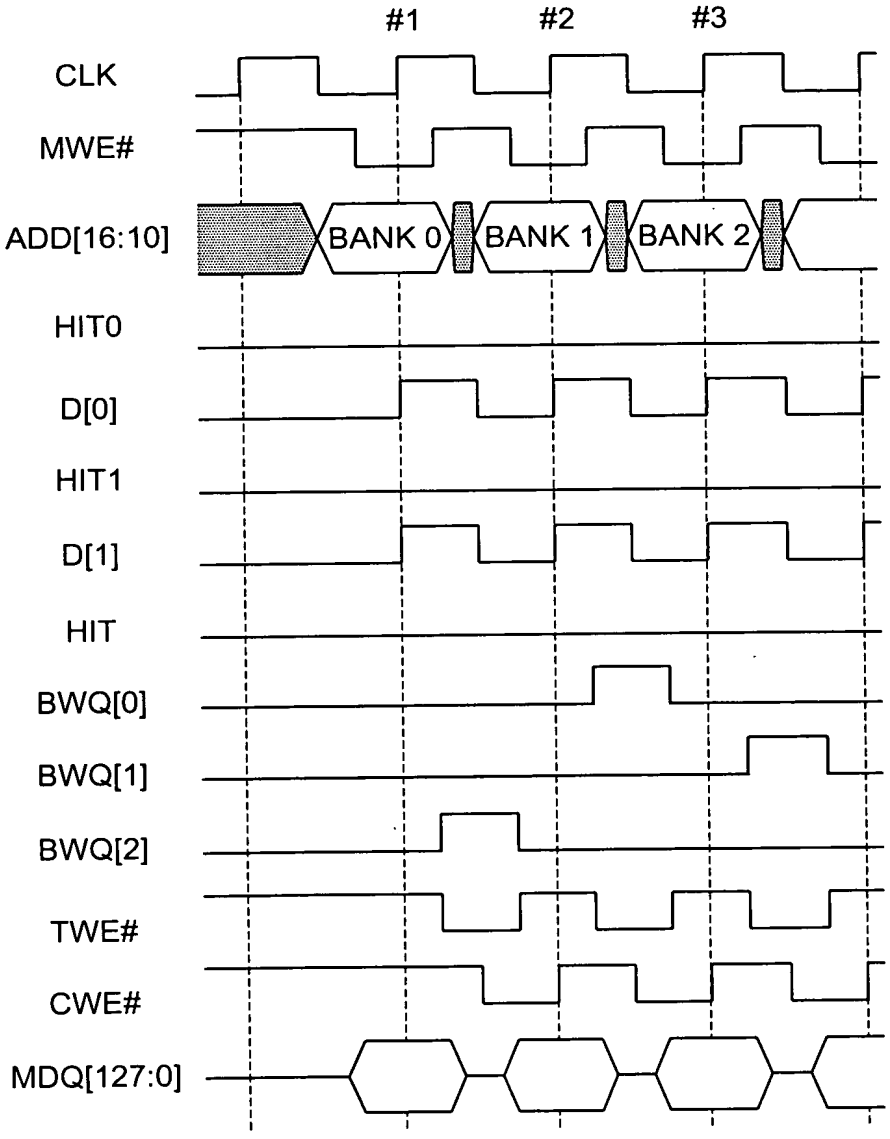

#1
#2
#3
CLK
MWE#
ADD[16:10]
BANK 0
BANK 1
BANK 2
HIT0
D[0]
HIT1
D[1]
HIT
BWQ[0]
BWQ[1]
BWQ[2]
TWE#
CWE#
MDQ[127:0]

FIG. 10

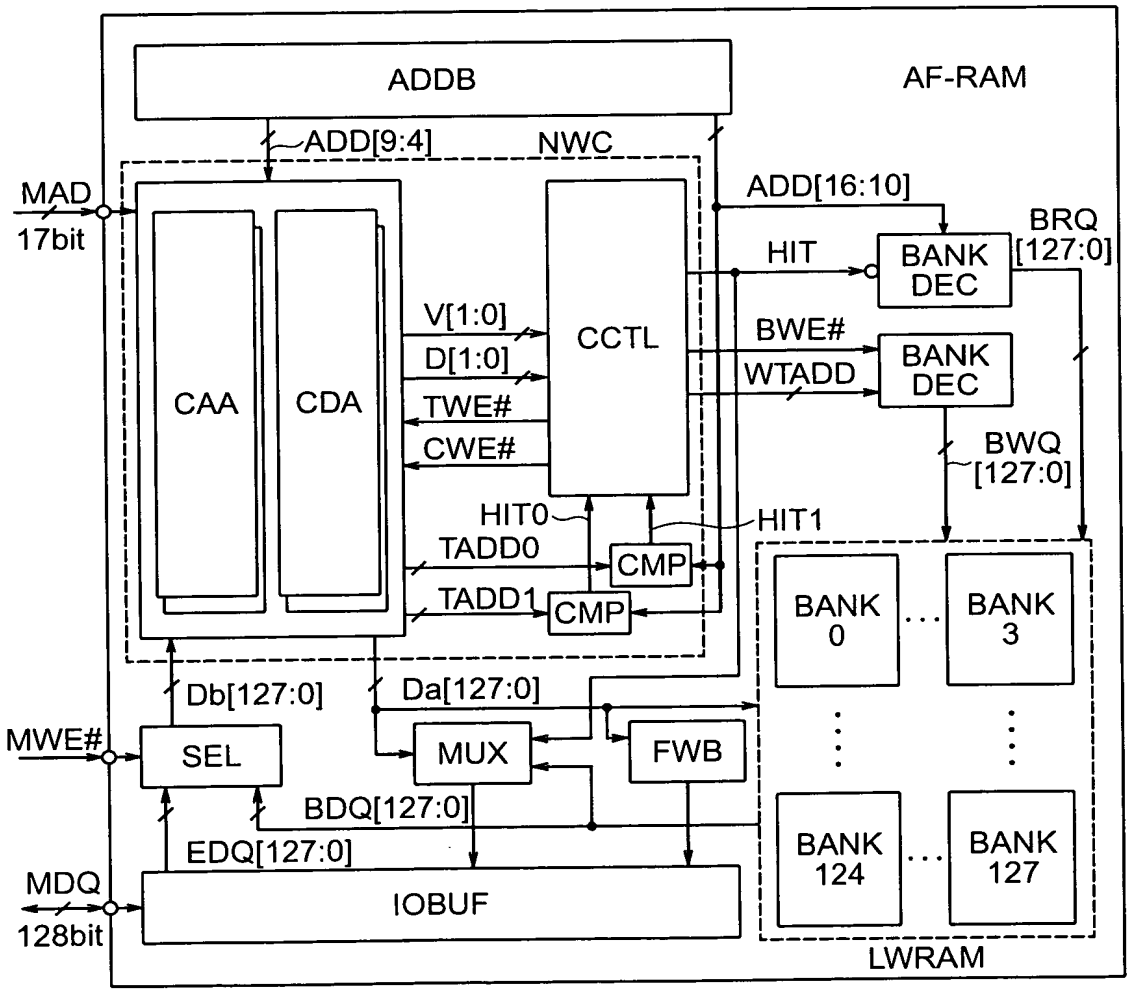

ADDB
AF-RAM
ADD[9:4]
NWC
MAD
17bit
ADD[16:10]
BRQ
[127:0]
HIT
BANK
DEC
CAA
CDA
V[1:0]
D[1:0]
TWE#
CWE#
CCTL
BWE#
WTADD
BANK
DEC
BWQ
[127:0]
HIT0
HIT1
TADD0
CMP
TADD1
CMP
BANK
0
BANK
3
Db[127:0]
Da[127:0]
MWE#
SEL
MUX
FWB
BDQ[127:0]
EDQ[127:0]
BANK
124
BANK
127
MDQ
128bit
IOBUF
LWRAM

FIG. 11

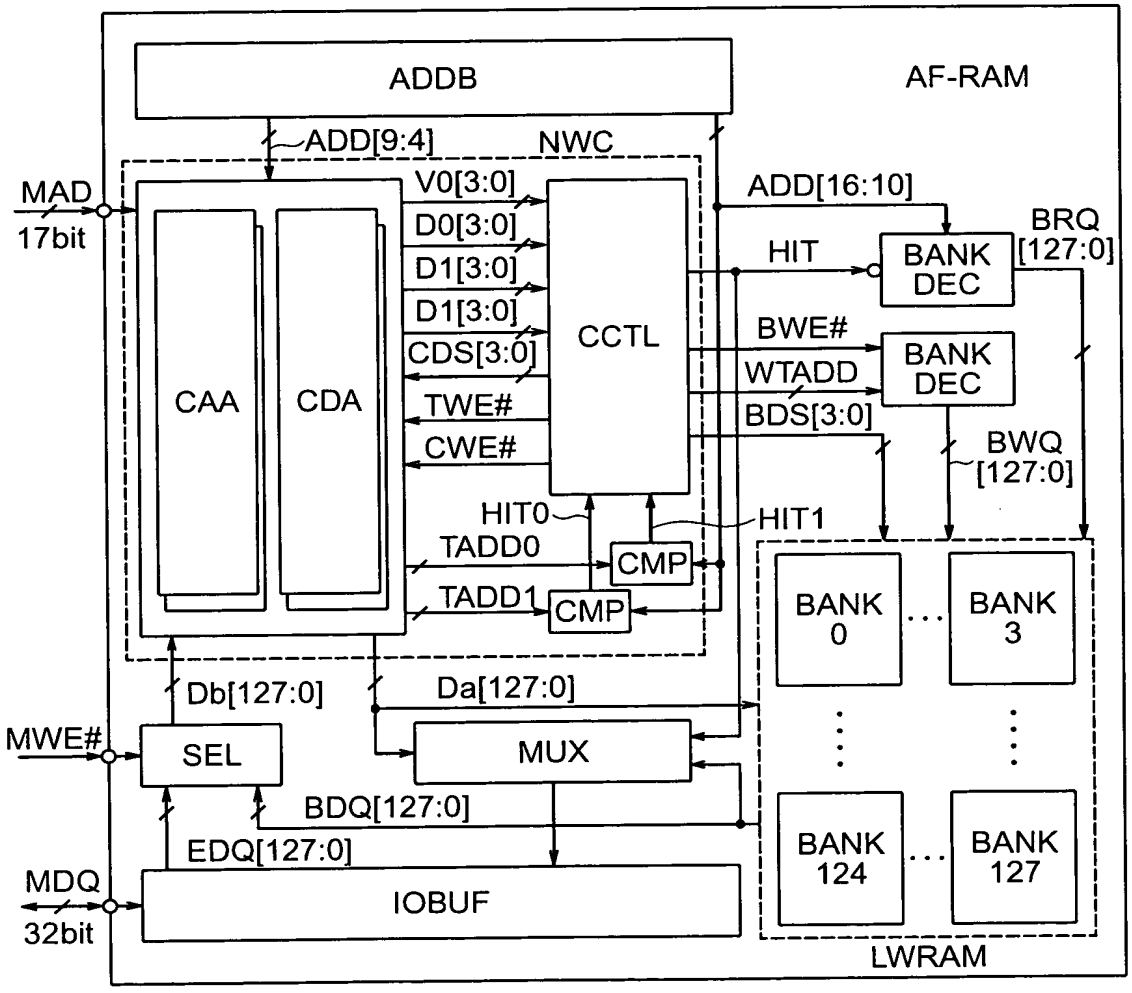

ADDB
AF-RAM
ADD[9:4]
NWC
MAD
17bit
V0[3:0]
D0[3:0]
D1[3:0]
D1[3:0]
CDS[3:0]
TWE#
CWE#
CAA
CDA
CCTL
ADD[16:10]
HIT
BANK DEC
BRQ [127:0]
BWE#
WTADD
BANK DEC
BDS[3:0]
BWQ [127:0]
HIT0
HIT1
TADD0
CMP
TADD1
CMP
BANK 0
BANK 3
Db[127:0]
Da[127:0]
MWE#
SEL
MUX
BDQ[127:0]
EDQ[127:0]
BANK 124
BANK 127
MDQ
32bit
IOBUF
LWRAM

FIG. 12

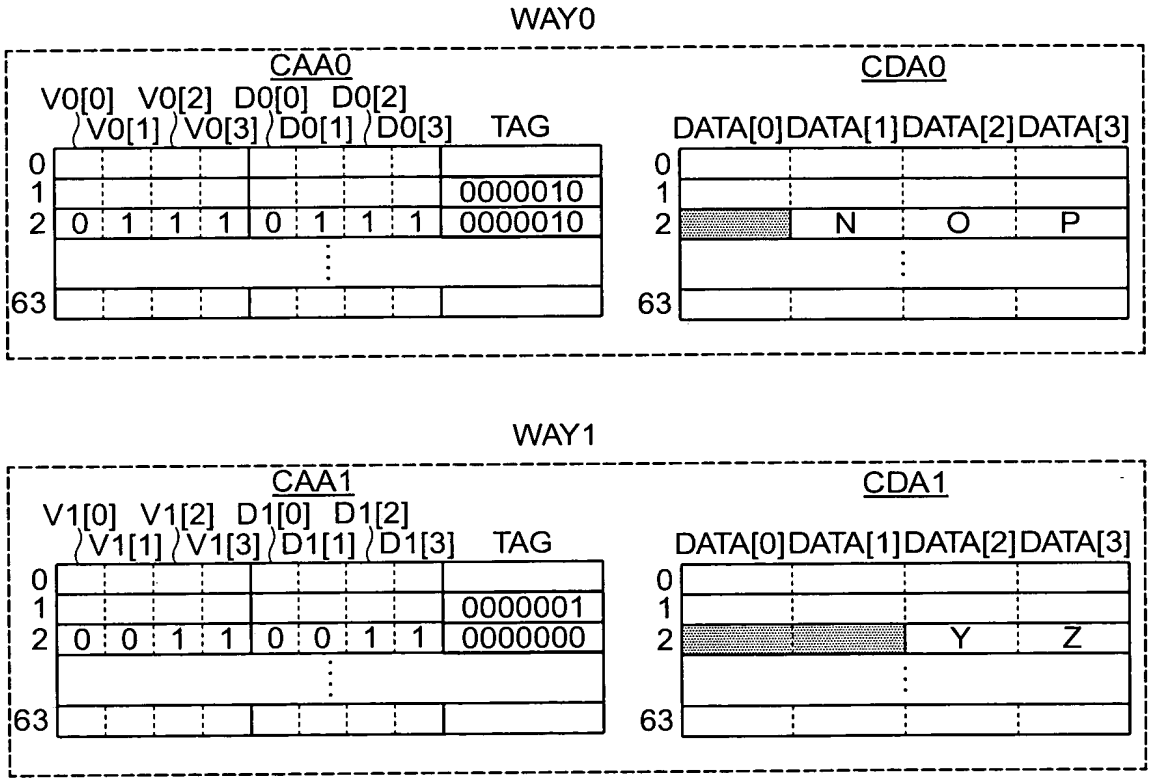

WAY0
CAA0
V0[0] V0[1] V0[2] V0[3] D0[0] D0[1] D0[2] D0[3] TAG
0
1
2 0 1 1 1 0 1 1 1 0000010
63
0000010
CDA0
DATA[0] DATA[1] DATA[2] DATA[3]
0
1
2 N O P
63
WAY1
CAA1
V1[0] V1[1] V1[2] V1[3] D1[0] D1[1] D1[2] D1[3] TAG
0
1
2 0 0 1 1 0 0 1 1 0000000
63
0000001
CDA1
DATA[0] DATA[1] DATA[2] DATA[3]
0
1
2 Y Z
63

FIG. 13

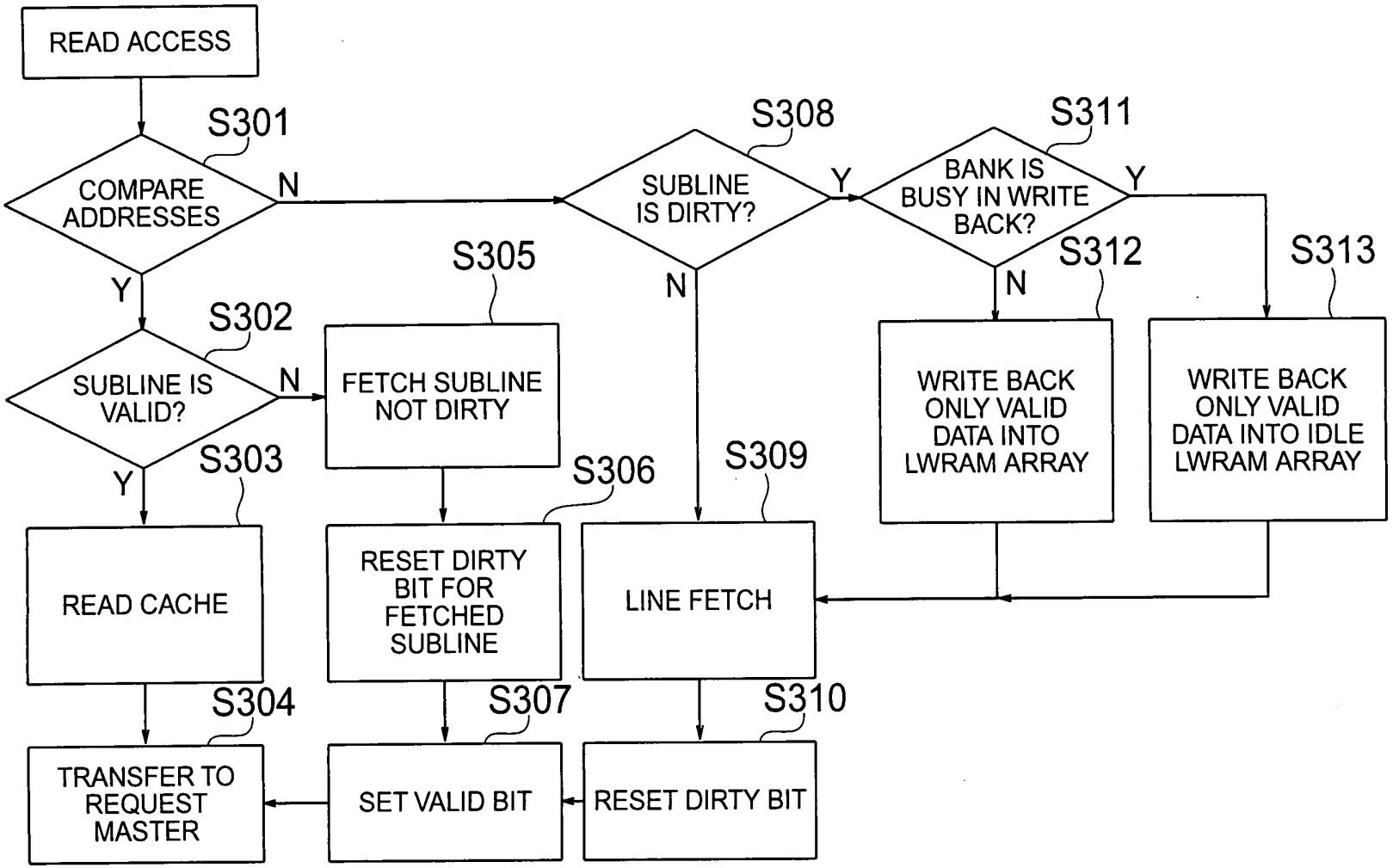

READ ACCESS
S301
COMPARE ADDRESSES
N
Y
S302
SUBLINE IS VALID?
N
Y
S303
READ CACHE
S304
TRANSFER TO REQUEST MASTER
S305
FETCH SUBLINE NOT DIRTY
S306
RESET DIRTY BIT FOR FETCHED SUBLINE
S307
SET VALID BIT
S308
SUBLINE IS DIRTY?
Y
N
S309
LINE FETCH
S310
RESET DIRTY BIT
S311
BANK IS BUSY IN WRITE BACK?
Y
N
S312
WRITE BACK ONLY VALID DATA INTO LWRAM ARRAY
S313
WRITE BACK ONLY VALID DATA INTO IDLE LWRAM ARRAY

FIG. 14

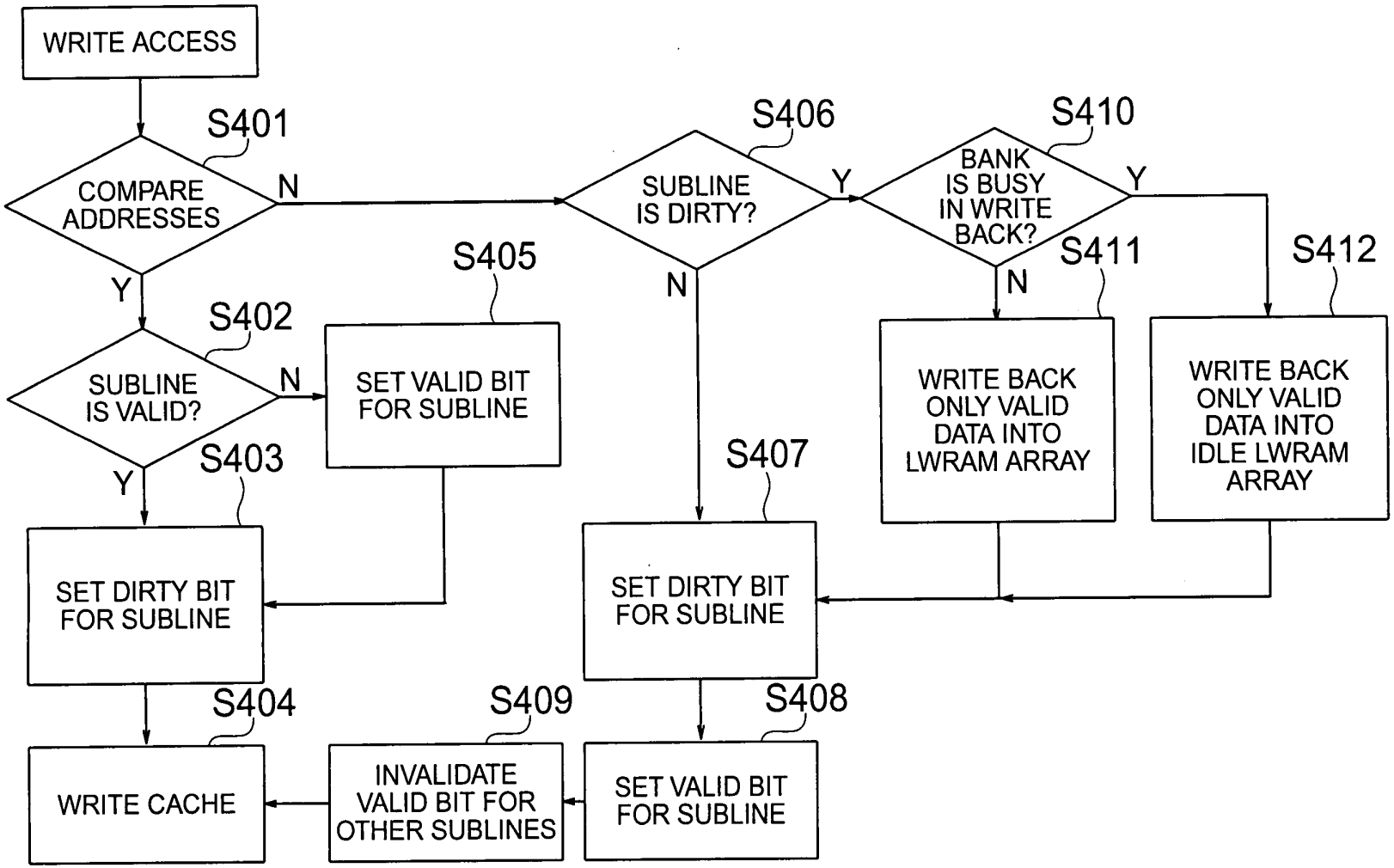

WRITE ACCESS
S401
COMPARE ADDRESSES
N
Y
S402
SUBLINE IS VALID?
N
Y
S403
SET DIRTY BIT FOR SUBLINE
S404
WRITE CACHE
S405
SET VALID BIT FOR SUBLINE
S406
SUBLINE IS DIRTY?
Y
N
S407
SET DIRTY BIT FOR SUBLINE
S408
SET VALID BIT FOR SUBLINE
S409
INVALIDATE VALID BIT FOR OTHER SUBLINES
S410
BANK IS BUSY IN WRITE BACK?
Y
N
S411
WRITE BACK ONLY VALID DATA INTO LWRAM ARRAY
S412
WRITE BACK ONLY VALID DATA INTO IDLE LWRAM ARRAY

FIG. 15

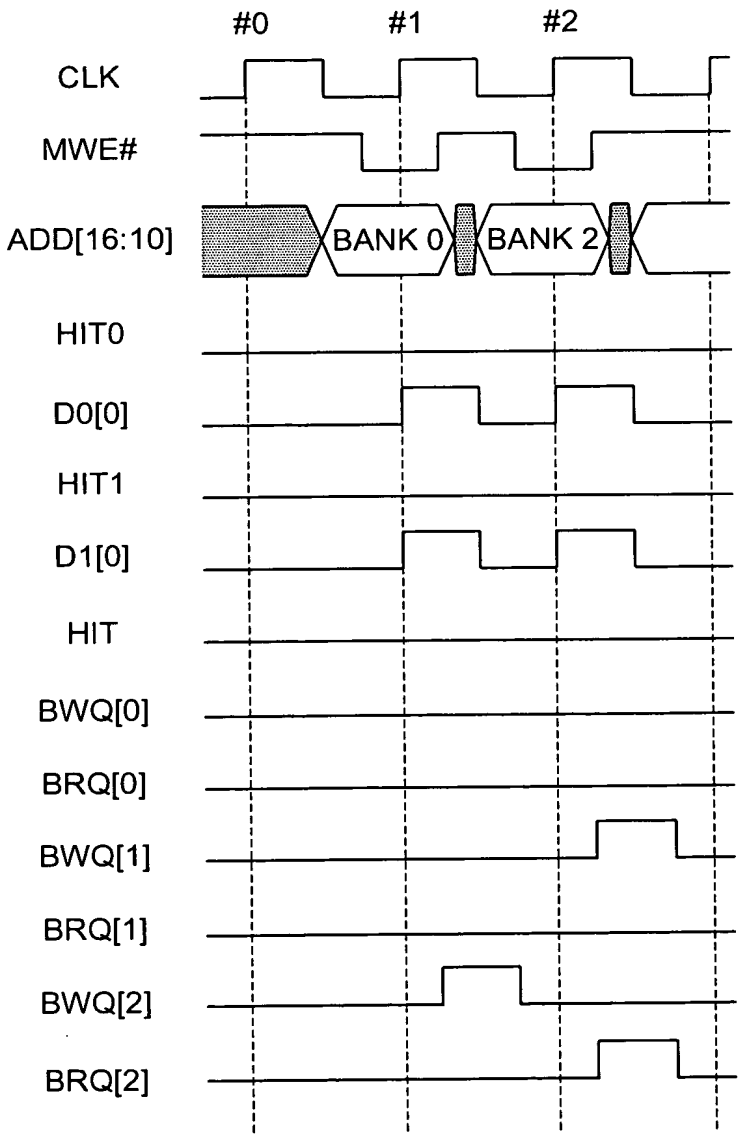

#0
#1
#2
CLK
MWE#
ADD[16:10]
BANK 0
BANK 2
HIT0
D0[0]
HIT1
D1[0]
HIT
BWQ[0]
BRQ[0]
BWQ[1]
BRQ[1]
BWQ[2]
BRQ[2]

FIG. 16

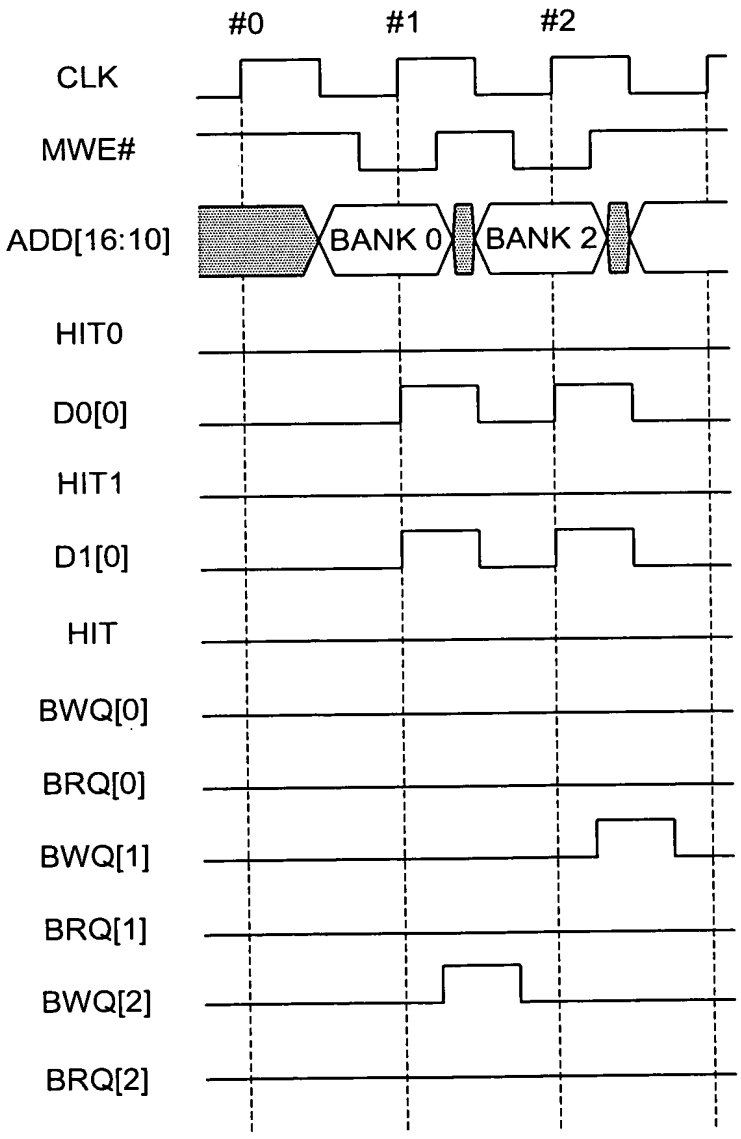

#0
#1
#2
CLK
MWE#
ADD[16:10]
BANK 0
BANK 2
HIT0
D0[0]
HIT1
D1[0]
HIT
BWQ[0]
BRQ[0]
BWQ[1]
BRQ[1]
BWQ[2]
BRQ[2]

FIG. 17

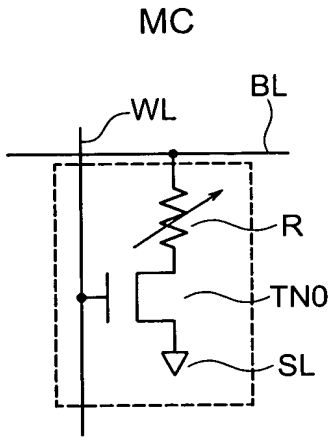


FIG. 18A

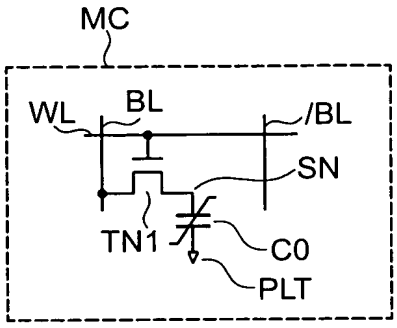


FIG. 18B

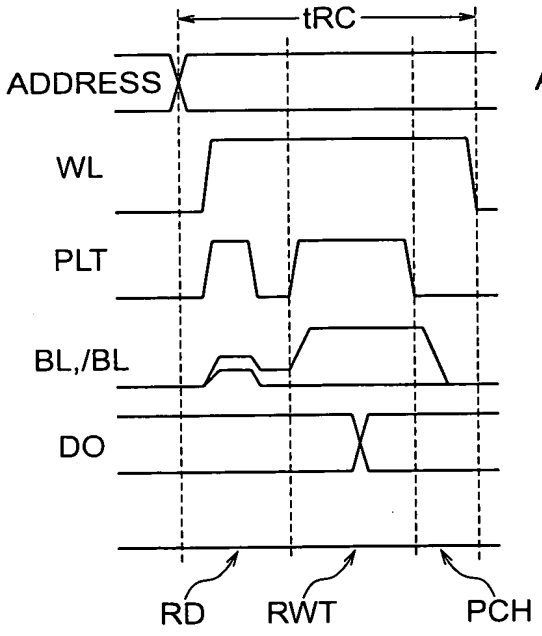


FIG. 18C

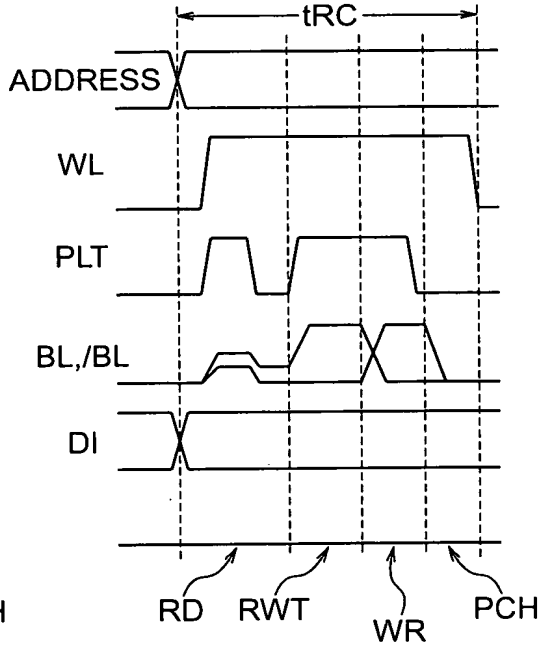


FIG. 19A

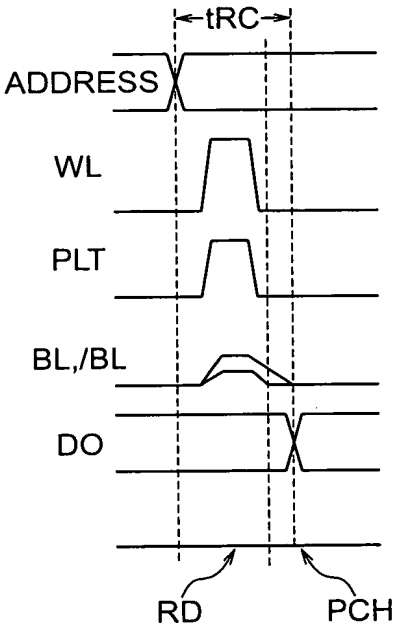


FIG. 19B

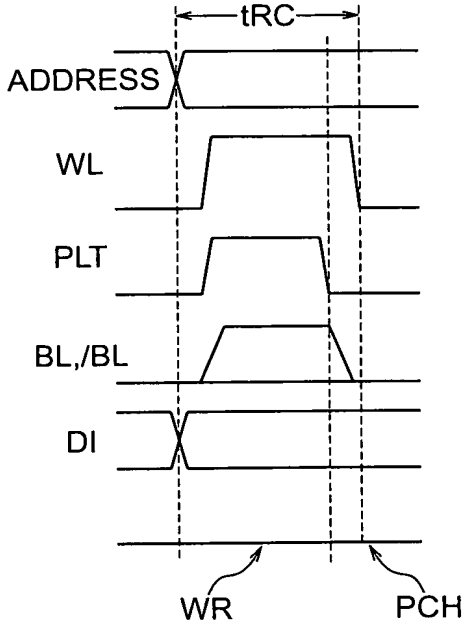


FIG. 20